APPENDIX B

Appendix B presents the performance requirements of IPC-6012C in an abbreviated form and alphabetical order. Special conditions, lengthy requirements, and tutorial information may be shortened or partially omitted in this appendix. See the referenced paragraph in this appendix for the full specification requirements.

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Etched Annular Ring (External PTHs)	Not greater than 180° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed.	The minimum annular ring **shall** be 50 µm [1,969 µin].	3.4.2 and Table 3-8
Etched Annular Ring (External Unsupported Holes)	Not greater than 90° breakout of hole from land when visually assessed.		The minimum annular ring **shall** be 150 µm [5,906 µin].	3.4.2 and Table 3-8
Etched Annular Ring (Internal PTHs)	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	The minimum internal annular ring **shall** be 25 µm [984 µin].	3.6.2.9 and Table 3-8
Bow and Twist	Maximum of 0.75% for surface mount printed boards and 1.5% for all other printed board technologies.			3.4.3
Burrs and Nodules	Allowed if minimum hole diameter is met.			Table 3-9
Cap Plating of Filled Holes	When cap plating of the filled via is specified on the procurement documentation, voids over the resin fill are not allowed. Visually discernable depressions (dimples) and protrusions (bumps) over via fill are acceptable providing they meet the requirements of Table 3-10.			3.5.4.8 and 3.6.2.11.2
Circuit Repair	No more than two repairs for each 0.09 m^2 [0.969 ft^2]; no impedance or minimum electrical spacing req. violated.			3.11.1
Circuits/PTH Shorts to Metal Substrates	The printed board **shall** be capable of withstanding 500 volts (DC) +15, -0 between circuitry/PTHs and the metal core substrates. There **shall** be no flashover or dielectric breakdown.			3.8.3
Cleanliness	Testing in accordance to IPC-TM-650, Method 2.3.25, with contamination level not greater than an equivalent of 1.56 µg/cm^2 of sodium chloride.			3.9.1
Coefficient of Thermal Expansion	If have metal cores/reinforcements with a req. to constrain thermal expansion in planar directions, CTE **shall** be within ± 2 ppm/°C for CTE and temp range spec on master drawing; testing w/ strain gauge method, according to IPC-TM-650, Method 2.4.41.2. Other methods of determining the CTE **shall** be AABUS.			3.10.7
Color Variations in Bond Enhancement Treatment	Mottled appearance/color variation accept; Random missing areas of treatment **shall** not be >10%.			3.3.2.9
Conductor Definition	Meet visual and dimension req., pattern and thickness as specified in procurement documentation.			3.5
Conductor Imperfections	30% of minimum specified in 10% of length or 25 mm [0.984 in], whichever is less.	20% of minimum specified in 10% of length or 13 mm [0.512 in], whichever is less.		3.5.3
	No cracks, splits or tears.			
Conductor Spacing	Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced an additional 30% due to processing, if not specified.		Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced an additional 20% due to processing, if not specified.	3.5.2
Conductor Surfaces				3.5.4
Conductor Thickness	If not specified, minimum conductor thickness **shall** be in accordance with 3.6.2.12 and 3.6.2.13.			3.5.1
Conductor Thickness Reduction	Reduction of conductor thickness not >30% of minimum.	Reduction of conductor thickness not >20% of minimum.		3.5.3.2
Conductor Width	If not specified, minimum conductor width **shall** be 80% of conductor pattern			3.5.1

Conductor Width Reduction	Reduction of conductor width not >30% of minimum.	Reduction of conductor width not >20% of minimum.		3.5.3.1
Copper Purity Elongation and Tensile Strength	Purity **shall** be no less than 99.5% pure, tensile strength not less than 36,000 PSI [248 MPa], elongation not less than 12%.			3.2.6.2
Copper Wrap Plating	Copper wrap plating minimum as specified in Table 3-2 **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required. Reduction of surface wrap copper plating by processing resulting in insufficient wrap plating is not allowed (see Figure 3-18).			3.6.2.11.1
Cracks, Barrel/Corner	None allowed for Class 1, 2 and 3.			Table 3-9
Cracks, External Foil	Allowed if cracks do not extend into plating.			Table 3-9
Cracks, Internal Foil	"C" cracks allowed on only one side of hole provided cracks do not extend through foil thickness.	None allowed.		Table 3-9
Cracks, Laminate	Boundary line cracks that overlap Zone A and Zone B or are entirely in Zone B shall not be greater than 150 µm [5,906 µin].	Boundary line cracks that overlap Zone A and Zone B or are entirely in Zone B shall not be greater than 80 µm [3,150 µin].		3.6.2.4
	Cracks between two uncommon conductors in either horizontal or vertical direction **shall** not decrease the minimum dielectric spacing.			
Crazing	Imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the distance of crazing **shall** not span more than 50% of the distance between adjacent conductors.			3.3.2.2
Delamination/Blistering (Visual)	Acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the printed board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the blister or delamination **shall** not span more than 25% of the distance between adjacent conductive patterns.			3.3.2.3
Delamination or Blistering	If present evaluate entire printed board per 3.3.2.3.	No evidence of delamination or blistering.		3.6.2.5
Dewetting	Solder connection: 15%.	Solder connection: 5%.		3.5.4.5
	Conductors and planes are permitted.			
Dielectric Thickness	The minimum dielectric spacing **shall** be specified in the procurement documentation. If the minimum dielectric spacing and the number of reinforcing layers are not specified, the minimum dielectric spacing **shall** be 90 µm [3,543 µin] and the number of reinforcing layers **shall** be selected by the supplier to ensure the minimum dielectric spacing.			3.6.2.15
Dielectric Withstand Voltage	No requirement.	Spacing 80 µm [3,150 µin] or greater, 500 Vdc Time: 30 sec (+3, -0) Spacing less than 80 µm [3,150 µin], 250 Vdc Time: 30 sec (+3, -0)		3.8.1 and Table 3-14
Dimensional Requirements	AABUS.			3.4
Edge Printed Board Contact, Junction of Gold Plate to Solder	Copper: 2.5 mm [0.0984 in]	Copper: 1.25 mm [0.04921 in]	Copper: 0.8 mm [0.031 in]	3.3.8
Edge Printed Board Contact, Junction of Gold Plate	Gold: 2.5 mm [0.0984 in]	Gold: 1.25 mm [0.04291 in]	Gold: 0.8 mm [0.031 in]	3.3.8

Edge Connector Lands	No cuts or scratches that expose nickel or copper; Pits, dents, or depressions accept if not exceed 0.15 mm [0.00591 in] in longest dimension with no more than three per land, and not appear in >30% of lands.			3.5.4.4
Edges (Visual)	Nicks or haloing do not penetrate more than 50% of distance from edge to nearest conductor or 2.5 mm [0.0984 in], whichever is less.			3.3.1
Electrical Requirements				3.8
Electrical Continuity and Isolation	Testing conducted in accordance with IPC-9252.			3.8.2
Etchback (When Specified)	Between 5 µm [197 µin] and 80 µm [3,150 µin] with a preferred depth of 13 µm [512 µin]. Shadowing is permitted on one side of each land. The combination of dielectric removal from etchback, wicking and random tears or drill gouges resulting from hole formation and/or hole cleaning **shall** not exceed the sum of the maximum allowable etchback and the maximum allowable wicking.			3.6.2.6
Final Finish Coverage (Areas not to be Soldered)	Exposed copper on areas not to be soldered is permitted on 1% of the conductor surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor edges.			3.5.4.7.1
Foreign Inclusions	Translucent and other particles acceptable provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in			3.3.2.4
Fungus Resistance	No fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.			3.10.3
Haloing	Does not penetrate more than 2.5 mm [0.0984 in] or 50% of distance to closest conductor, whichever is less.			3.3.1
Hole Size and Hole Pattern Accuracy	AABUS. Applicable design series requirements **shall** apply if not specified.			3.4.1
Impedance Testing	Requirements for impedance **shall** be AABUS. The TDR (Time Domain Reflectometer) technique in accordance with IPC-TM-650, Method 2.5.5.7 may be used to perform impedance testing on a test coupon or a designated circuit in the production printed board.			3.10.6
Inclusions, Innerlayer (Inclusions Between Interface of Internal Land and Through-Hole Plating)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.		Table 3-9
Insulation Resistance (As Received)	As received: Maintain electrical function.	As received: 500 megohms.		3.10.9 and Table 3-5
	After exposure to moisture: Maintain electrical function.	After exposure to moisture: 100 megohms.	After exposure to moisture: 500 megohms.	3.8.4 and Table 3-5
Laminate Integrity	See Voids, Laminate.			3.6.2.3
Lifted Lands	Lifted lands are allowed on the thermally stressed microsection.			3.6.2.10
Lifted Lands (Visual)	No lifted lands on the delivered (non-stressed) printed board.			3.3.4
Marking (Visual)	Conductive marking must be compatible with materials, and not reduce electrical spacing requirements. For lead-free end product, the labeling requirements of J-STD-609 **shall** be met.			3.3.5
Material				3.2
Measling	Measling is acceptable for Class 1, Class 2 and Class 3 end product. Measled areas in laminate substrates exceeding 50% of the spacing between non-common conductors are a process indicator for Class 3 end product, indicating a variation in material, equipment operation, workmanship or process that is not a defect.			3.3.2.1
Mechanical Shock	Printed board **shall** pass test requirements of 3.8.2 after mechanical shock.			3.10.5
Metal Cores, Horizontal Microsection	Wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material **shall** not reduce electrical spacing between adjacent conductive surfaces to <0.100 mm [0.00394 in]. Wicking and/or radial cracks **shall** not exceed 75 µm [2,953 µin] from the PTH edge into the hole-fill.			3.10.10
Metal Core, Internal Spacing	The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or PTHs **shall** be 100 µm [3,937 µin].			3.6.2.14

Minimum Internal Layer, Copper Foil Thickness	See Table 3-11.			3.6.2.12
Minimum Surface Conductor Thickness	See Table 3-12.			3.6.2.13
Moisture and Insulation Resistance	No measling, blistering or delamination in excess of that allowed in 3.3.2; insulation resistance meet requirements of Table 3-15; moisture and insulation resistance testing according to IPC-TM-650, Method 2.6.3.			3.8.4
Nail Heading	Acceptable			3.6.2.17
Negative Etchback	Distance “X” not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.		Distance “X” not to exceed 13 µm [512 µin] if etchback not specified on procurement documentation.	3.6.2.8 and Figure 3-12
	Distance “Z” not to exceed 37.5 µm [1,476 µin] if etchback not specified on procurement documentation.		Distance “Z” not to exceed 19.5 µm [768 µin] if etchback not specified on procurement documentation.	
	When negative etchback results in folds or inclusions in the copper plating, the copper thickness **shall** meet the minimum requirements as measured from the face of the internal layer as shown in Figure 3-8.			
Nicks and Pinholes in Ground or Voltage Planes	Maximum size 1.5 mm [0.0591 in] with not more than six per side, per 625 cm^2	Maximum size 1.0 mm [0.0394 in] with not more than four per side, per 625 cm^2.		3.5.4.1
Nonwetting	For tin, tin/lead reflowed, or solder coated surfaces, not permitted on any conductive surface where a solder connection will be required.			3.5.4.6
Organic Contamination	Tested according to IPC-TM-650, Method 2.3.38 or 2.3.39, with no positive visual ID of organic contamination.			3.10.2
Outgassing	Testing in accordance to procurement documentation; not resulting in a weight loss of more than 0.1%.			3.10.1
Pink Ring	Acceptable.			3.3.2.10
Plating Adhesion	No portion of protective plating or conductor pattern foil **shall** be removed. Testing in accordance with IPC-TM-650, Method 2.4.1.			3.3.7
Plating Folds, Inclusions	The minimum copper thickness in Table 3-2 must be met. For positive etchback, measurements should follow the topography of the dielectric. When negative etchback results in folds in the copper plating, the copper thickness **shall** meet the minimum requirements as measured from the face of the internal layer (see Figure 3-8); negative etchback limits **shall** not be exceeded.			Table 3-9
Plating Integrity, PTHs	Properties specified in Table 3-9.			3.6.2.1
Plating Thickness, Copper, Blind Vias > 2 layers	Avg. 20 µm [787 µin] Min. Thin areas 18 µm [709 µin]		Avg. 25 µm [984 µin] Min. Thin areas 20 µm [787 µin]	3.6.2.11, Table 3-3
Plating Thickness, Copper, Blind and Buried Microvias	Avg. 12 µm [472 µin] Min. Thin areas 10 µm [394 µin]			3.6.2.11, Table 3-4
Plating Thickness, Copper, Buried Via Cores (2 layers)	Avg. 13 µm [512 µin] Min. 11 µm [433 µin]	Avg. 15 µm [592 µin] Min. Thin areas 13 µm [512 µin]		3.6.2.11, Table 3-5
Final Finish and Coating Thickness	See Table 3-2.			3.6.2.11, Table 3-2
Plating and Coating Voids in the Hole (Visual)	Copper: three voids per hole in <10% of holes.	Copper: one void per hole in < 5% of holes.	Copper: none.	3.3.3
	Finished Coating: five voids per hole in not more than 15% of holes.	Finished Coating: three voids per hole in not more than 5% of holes.	Finished Coating: one void per hole in not more than 5% of holes.	
	Areas of contamination or inclusions not to exceed 5% of each side of the interconnection or occur in the interface of the copper cladding on the core and the copper plating in the hole wall.			

Plating Voids	Meet requirements established in Table 3-9.	No more than one void per specimen, regardless of length or size. No plating void in excess of 5% of total printed board thickness. No plating voids evident at internal layer and PTH hole wall interface. No circumferential plating voids greater than 90°.	3.6.2.2
Repair	AABUS. The repairs **shall** be in accordance with IPC-7711/21.		3.11
Material Fill of Blind and Buried Vias	Fill material in a blind via with an aspect ratio greater than 1:1 **shall** be 60% minimum for Class 2 and Class 3 or as specified in the procurement documentation. Fill material within the blind via **shall** be planar with the surface within +/- 0.076 mm [0.003 in] unless otherwise specified. When cap plating is specified, fill material within the blind via **shall** meet the dimple/bump requirements of Table 3-10. Buried vias **shall** be at least 60% filled with the laminating resin or similar via filling material for Class 2 and Class 3. They may be completely void of fill material for Class 1.		3.6.2.16
Rework	Does not affect functional integrity of printed board.		3.12
Scratches, Dents, and Tool Marks	Do not bridge conductors or expose fibers greater than that allowed in 3.3.2.4 and 3.3.2.5, and do not reduce dielectric spacing below minimum.		3.3.2.7
Separation Along Vertical Edge of External Land	Allowed at knee (see Figure 3-7), maximum length 130 µm [5, 118 µin].	Allowed provided the separation does not extend beyond the vertical edge of the external copper foil.	Table 3-9
Separation, Innerlayer (Separation at the Interface Between Internal Lands and Through-Hole Plating	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	Table 3-9
Separation, Plating	None allowed.		Table 3-9
Smear Removal	Smear removal **shall** be sufficient to meet the acceptability criteria for innerlayer separation per Table 3-9. Smear removal **shall** not include the lateral removal of resin greater than 25 µm [984 µin]; random tears or drill gouges which produce small areas where the 25 µm [984 µin] depth is exceeded **shall** not be evaluated as smear removal.		3.6.2.7
Solder Mask			3.7
Solder Mask Coverage	Conductors not to be exposed or bridged by blisters in solder mask areas. For exposed dielectric, encroachment on lands, blistering, pits and voids in dielectric areas and printed board edge chipping, see 3.7.1.		3.7.1
Solder Mask Cure and Adhesion	No tackiness, delamination or blistering; maximum loss of adhesion after tape test per Table 3-13.		3.7.2
Solderability (Visual)	Solderability testing and accelerated aging will be in accordance to J-STD-003.		3.3.6
Special Requirements (When Specified)	AABUS.		3.10
Structural Integrity	**Shall** meet structural integrity requirements for thermally stressed evaluation coupons specified in 3.6.2.		3.6
Surface Microvoids	Not exceed 0.8 mm [0.0315 in] in longest dimension, bridge conductors, nor exceed 5 % of printed board area per side.		3.3.2.8
Solderable Surface Mount Lands (Rectangular)	Defects along edge of land not >30%; internal defects not >20%.	Defects along edge of land not >20%; internal defects not >10%.	3.5.4.2.1
	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. One electrical test probe mark allowed within the pristine area for Class 1, 2 and 3.		
Solderable Surface Mount Lands (Round)	Defects along edge of land do not radially extend towards center by more than 30% of the diameter of the land and not extend more than 30% around the circumference of the land.	Defects along edge of land do not radially extend towards center by more than 20% of the diameter of the land and not extend more than 20% of the circumference of the land.	3.5.4.2.2

	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. One electrical test probe mark allowed within the pristine area for Class 1, 2 and 3.			
Thermal Shock	When specified, testing/evaluation according to IPC-TM-650, Method 2.6.7.2, with temp range between -65 to 125 °C [-85 to 257 °F]. An increase in resistance of 10% or more **shall** be considered a reject and **shall** meet requirements of Table 3-9 after cycling.			3.10.8
Thermal Stress Testing	Test coupons or production printed boards **shall** be thermally stressed. Per the applicable criteria listed in 1.3.3, one or more of the following Test Methods **shall** be required: **3.6.1.1 Thermal Stress Testing, Method 2.6.8**. **3.6.1.2 Thermal Stress Testing, Method 2.6.27 (230 °C)** **3.6.1.3 Thermal Stress Testing, Method 2.6.27 (260 °C)**			3.6.1
Vibration	Printed board **shall** pass test requirements of 3.9.2 after vibration cycling.			3.10.4
Visual	Finished product **shall** be examined, be of uniform quality, and conform to 3.3.1 through 3.3.9.			3.3
Voids, Laminate	Boundary line voids that overlap Zone A and Zone B or are entirely in Zone B are not >150 µm [5,906 µin].	Boundary line voids that overlap Zone A and Zone B or are entirely in Zone B are not > 80 µm [3,150 µin].		3.6.2.3
Voids in Surface	Acceptable if not > 0.8 mm [0.031 in] in longest dimension or exceed 5% of the printed board area per side.			3.3.2.8
Weave Exposure	Weave exposure does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum.		No weave exposure.	3.3.2.5
Wicking	125 µm [4,921 µin] maximum	100 µm [3,937 µin] maximum	80 µm [3,150 µin] maximum	Table 3-9
Wire Bond Pads	Final conductor finish as specified in 1.3.4.3 for GWB-1, GWB-2 or ENIG. Final finish coating per Table 3-2 for applicable coating. Pristine area **shall** have maximum surface roughness of 0.8 µm [32 µin] RMS as measured in accordance with IPC-TM-650, Method 2.4.15. No pits, nodules, scratches, electrical test probe marks within the pristine area that violates RMS requirement.			3.5.4.3
Workmanship	**Shall** be free of defects and of uniform quality - no visual of dirt, foreign matter, oil, fingerprints.			3.3.9