ENGINEERING INPUT - NEW CIRCUIT BOARD DESIGN

TITLE		JOB NUM
ELEC ENGINEER	EXT	CHG NUM
MECH ENGINEER	EXT	SCH NUM
PROJECT LEAD	EXT	BRD NUM
DATE REC'D	CONTROL#	ASY NUM
DATE REQ	QTY NEEDED	MECH NUM

CHECKLIST

PRELIMINARY :

BOARD THICKNESS:

COPPER THICKNESS: _____

PROPOSED LAYER COUNT _____

- O BOARD OUTLINE: IMPORT FROM PRO/E
- O BOARD OUTLINE: INCLUDED IN FILES:
- O USE PREVIOUS PART NUM:

☐ PRODUCTION OR ☐ TEST ONLY

Y / N RECOMMENDED FLOOR PLAN

SCHEMATIC : PLEASE INDICATE IF POSSIBLE

- ☐ HIGH VOLTAGE / HIGH CURRENT
- ☐ HIGH SPEED LINES / IMPEDANCE CONTROL
- ☐ SIGNALS NEEDING SHIELDING OR ISOLATION
- ☐ IF MULTIPLE GNDS, SHOW COMMON RETURN
- ☐ ANY NET CLASSES, NET PROPERTIES IN SCH?
- ☐ UNUSED INPUTS TIED HIGH OR LOW

Y / N REORDER REFERENCE DESIGNATORS?

LAYOUT CONSIDERATIONS :

EXPLAIN IN NOTES (RIGHT COLUMN) OR ATTACH

Y / N HIGH VOLUME? COST SENSITIVE?

Y / N PALLETIZED FOR ASSEMBLY?

Y / N COMPONENT HEIGHT RESTRICTIONS?

Y / N COMPONENT KEEP-OUT AREAS?

Y / N EXTRA TEST POINTS? ACCESSIBILITY?

Y / N HEAT SINK REQUIREMENTS?

Y / N ANY NEED FOR THERMAL ANALYSIS?

Y / N ANY SIMULATION RESULTS (PSPICE)?

Y / N EMC ANALYSIS?

Y / N ORIENTATION EMULATORS/TEST/WAVE?

NOTES